Hall Ticket Number:

Code No. : 14405

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (CBCS: ECE) IV-Semester Main Examinations, May-2018

Pulse, Digital and Switching Circuits

Time: 3 hours Max. Marks: 70

*Note: Answer ALL questions in **Part-A** and any FIVE from **Part-B***

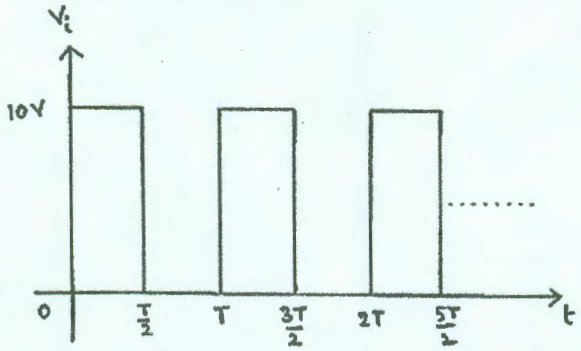
Part-A (10 × 2 = 20 Marks)

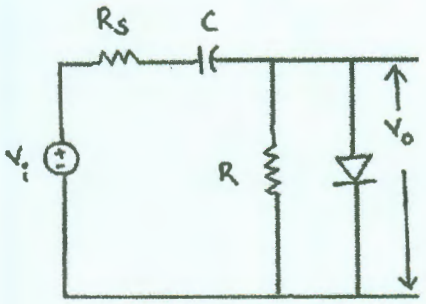
1. How does an RC Low Pass filter behaves when RC>>T? Write the output expression for LPF.
2. Draw a clipper circuit to allow the part of input sine wave if input is greater than 2V?
3. Write the applications of Schmitt trigger?
4. What are the drawbacks of direct coupled binary circuit?
5. Simplify the given boolean function
   F = A+AB+ABC+.....
6. Why NAND and NOR gates are known as universal gates? Justify.
7. Distinguish between combinational and sequential circuits.
8. Write the excitation tables for SR and JK Flip-Flops.
9. What is race around condition? When and why does it occur?
10. List out the architectural features of Mealy and Moore machines.

Part-B (5 × 10 = 50 Marks)

11. a) Explain the operation of Compensated attenuator. [5]

    b) A square wave with amplitude 10Volts and repetition frequency 10 kHz is applied to the following circuit with circuit parameters given by [5]
    $R_s = R_f = 100\Omega, R = 20K\Omega, C = 1\mu F, V_\gamma = 0.$





Determine the output voltage waveform for few cycles and indicate its voltage levels.

12. a) Explain the operation of emitter coupled binary circuit and derive the necessary expressions with a neat sketch. [6]

    b) Show that an astable multivibrator can be used as a voltage to frequency converter. [4]

13. a) Simplify the following Boolean expression for minimal POS form using K-map and implement using NOR gates. F(w, x, y, z) = πM(4,5,6,7,8, 12) + πd(1,2,3,9,11,14). [6]

    b) Minimize the given function using K-map and for minimized function draw its logic diagram using NAND gates. [4]
    F(a, b, c, d) = Σm (0, 1, 2, 3, 4, 8, 9, 12).

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14. a) Convert the following Flip-Flops [5]
    i) D to SR Flip- Flop ii) D to JK Flip- Flop.

    b) Implement the following function F (a, b, c, d) = Σm (0, 1, 2, 3, 4, 8, 9, 12). [5]
    Using i) 8×1 multiplexer ii) 4×1 multiplexer

15. a) Design a mod-6 synchronous counter using JK Flip-Flops. [7]

    b) List out the merits and demerits of one hot encoding. [3]

16. a) Derive an expression for frequency of UJT Relaxation Oscillator. [5]

    b) Explain the operation of High Pass RC circuit to an exponential input. [5]

17. Answer any ***two*** of the following:
    a) Full subtractor using only 2 input NAND gates [5]
    b) 4-bit adder/subtractor [5]
    c) 3-bit twisted ring counter [5]

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